SAAB
Challenges and Vision

CASTOR Inaugural Celebration

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September 12, 2018

Agenda

Vision for the future regarding software technology / development

- History at Saab
- Where we are, evolutionary trend
- Strategy, disruptive forecast
- Challenges/expectations on Castor

Introduction

Oak Tree

Power

Survival

Ancient Wisdom

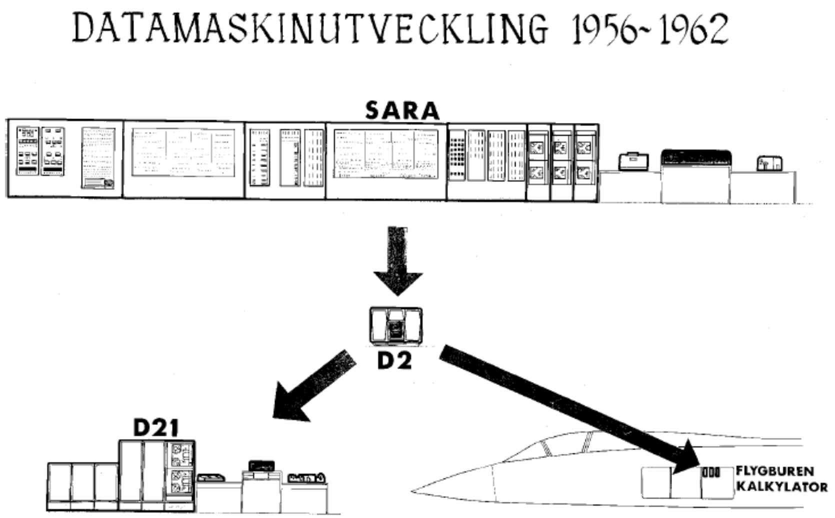
...

Forecast focus – Software technology needs

- **Determinism** : Identify and avoid or manage shared resources (used by software functions).
    - Refine allocation of partition/function to CPU, beyond ARINC 653 real time operative system.
    - Development of distributed software for parallell execution over network.
    - Network coding and software defined networking.
- **Security and Safety** : Are critical for cyber-physical systems. Although security and safety have traditionally been handled separately in the design process, cyber-physical systems cause interactions that require safety and security to be handled holistically.
- **Machine Learning** : Artificial intelligence is expected to escalate in cyber-physical systems.
- **Complexity wall** : Early understanding of the software system complexity contributes to reducing overall software costs and helps to estimate development time needed.
- **Executable Specification** : Specifications written in a formal language allow automated verification process starting early in the design process and at high abstraction levels without the need to code several new verification models; this enables an integrated design flow from specification to completed system that can be completely validated at each step.

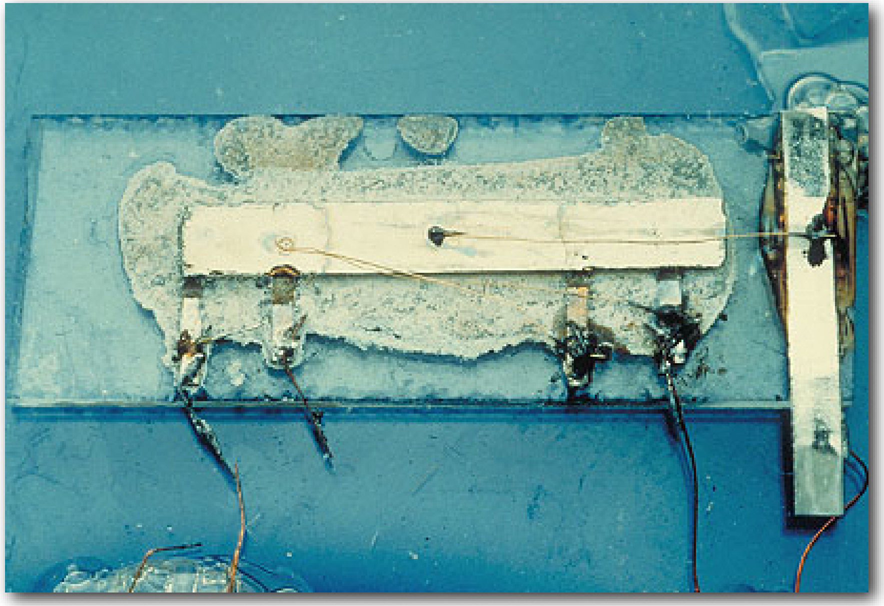
History

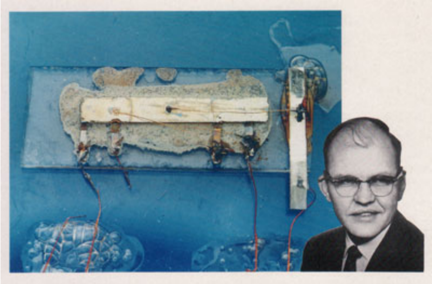
- 1948 – Swedish computer history begins with "Matematikmaskinnämnden"
- 1953 - Besk, "Binär elektronisk sekvens-kalkylator". Sweden's first electronic computer
- In May 1954, the "Matematikmaskinnämnden" appointed a course in programming, probably the first programming course in Sweden. The course lasted for six days with two hours of lectures and three to four hours of exercises daily. Then followed a few days of exercise on Besk
- Saab's computer was named Sara and came into operation in 1957



Ref: "Tema Flyg, Flygets Datorpionjärer", http://www.datasaab.se/Bok_1_5/book_2.htm
Ref: Gunnar Lindström, SAAB Flight-computer, https://www.youtube.com/watch?v=wn-ZsxTUevQ

Year 1958 – Invention of the integrated circuit





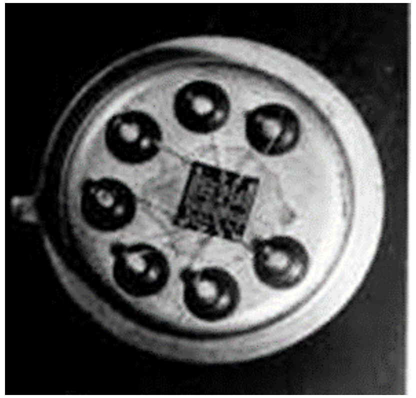
- Jack Kilby – Texas instrument – Nobel Prize Year 2000
- Robert Noyce – Fairchild Semiconductor – Patent No 2,981,877

Ref: Kilby, Jack St Clair. "Turning potential into realities: The invention of the integrated circuit (Nobel lecture)
Ref: Noyce, Robert N. "Semiconductor device-and-lead structure." U.S. Patent No. 2,981,877. 25 Apr. 1961.

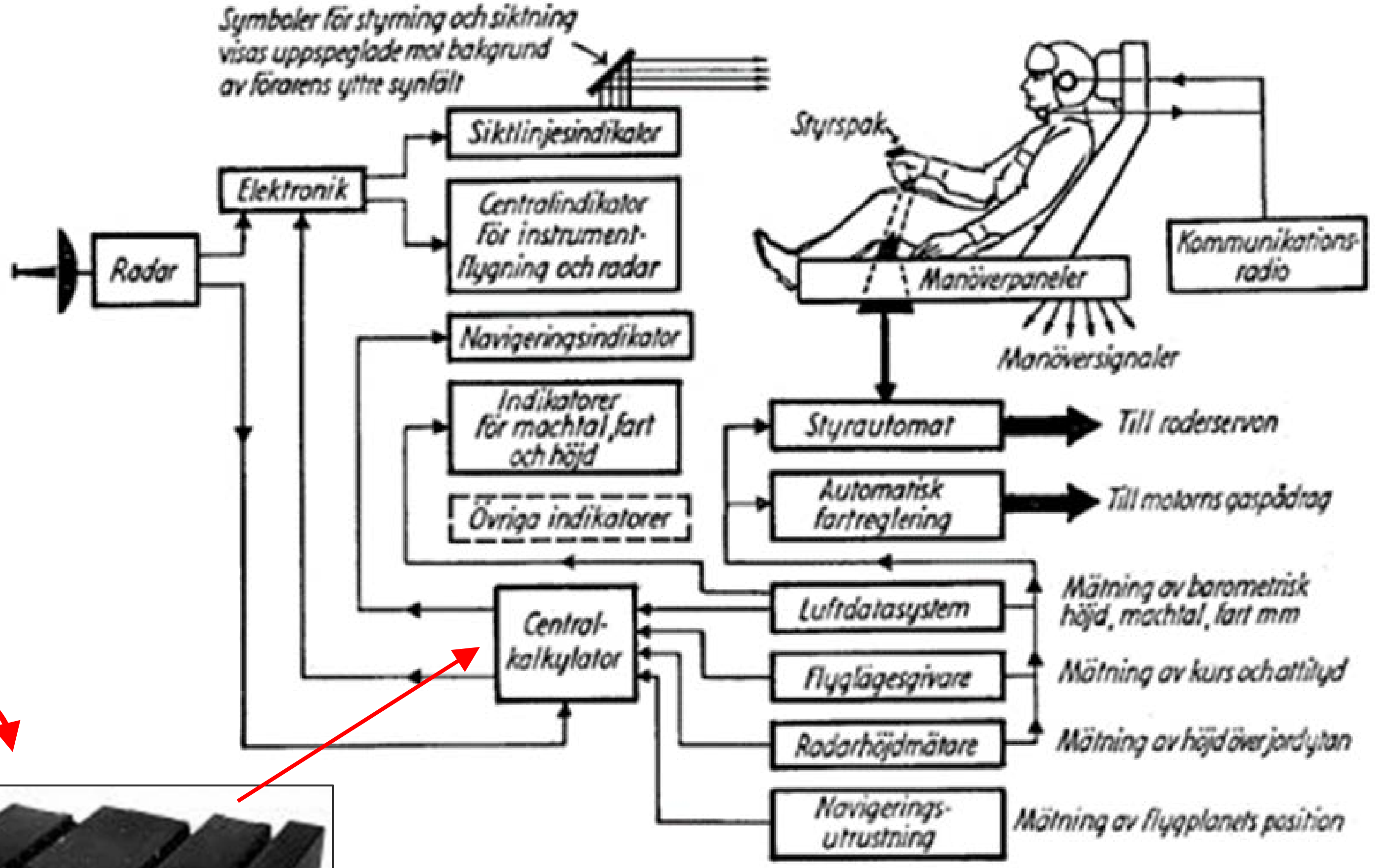
Year 1961 – First integrated circuit at Saab

- AJ37 – CK37 computer
- Typarbete 1961
- First flight 1967

Fairchild



CK37

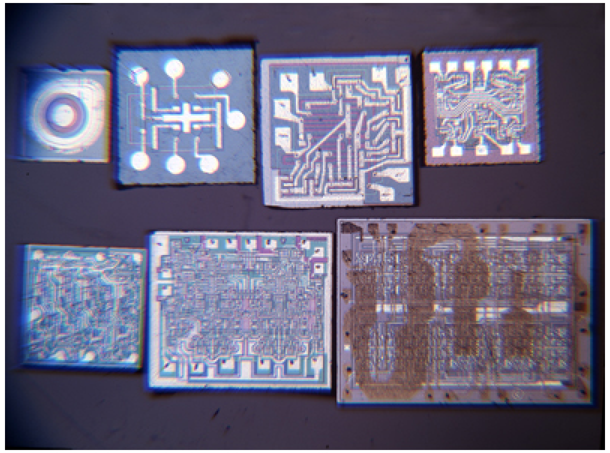


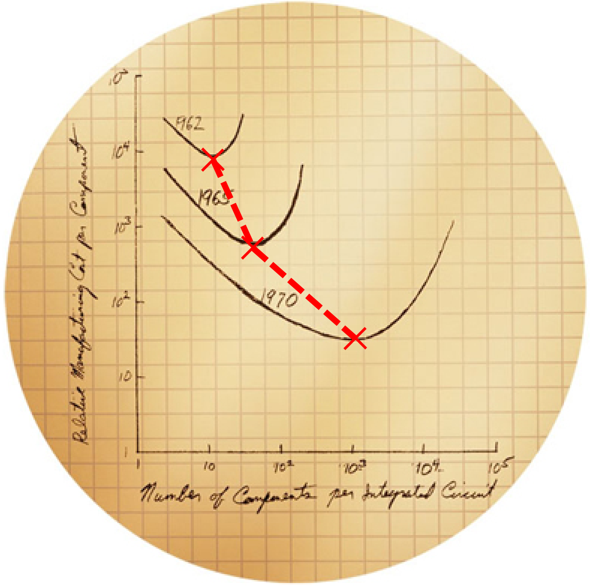
Ref: Jiewertz, Bengt. "Central Computer for aircraft Saab 37, Viggen."

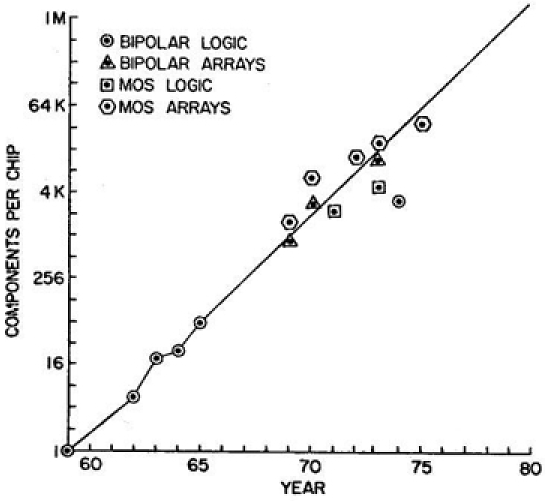
MOORE’S LAW – Manufacturing cost minimum

- ***Gordon E. Moore*** - Electronics, Volume 38, Number 8, April 19, 1965

  “Cramming more components onto integrated circuits”
- ***Robert Noyce (Bob)*** and ***Gordon*** found Intel (**Int**egrated **el**ectronics) 1968





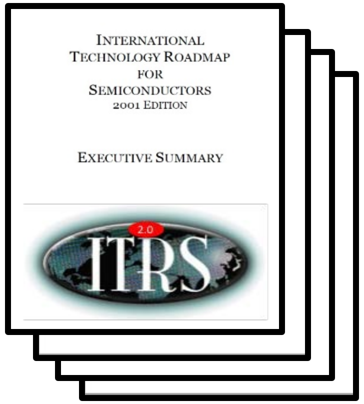


Ref: Moore, Gordon E. "Cramming more components onto integrated circuits, Reprinted from Electronics, volume 38, number 8, April 19, 1965
Ref: https://newsroom.intel.com/news/intel-50-gordon-moore-founding-intel/

The Global Route to Future …

- 1992 – Semiconductor Industry Association (SIA) coordinated the first *National Technology Roadmap for Semiconductors* (*NTRS*)

The International Technology Roadmap for Semiconductors (ITRS) is the result of a worldwide consensus building process.



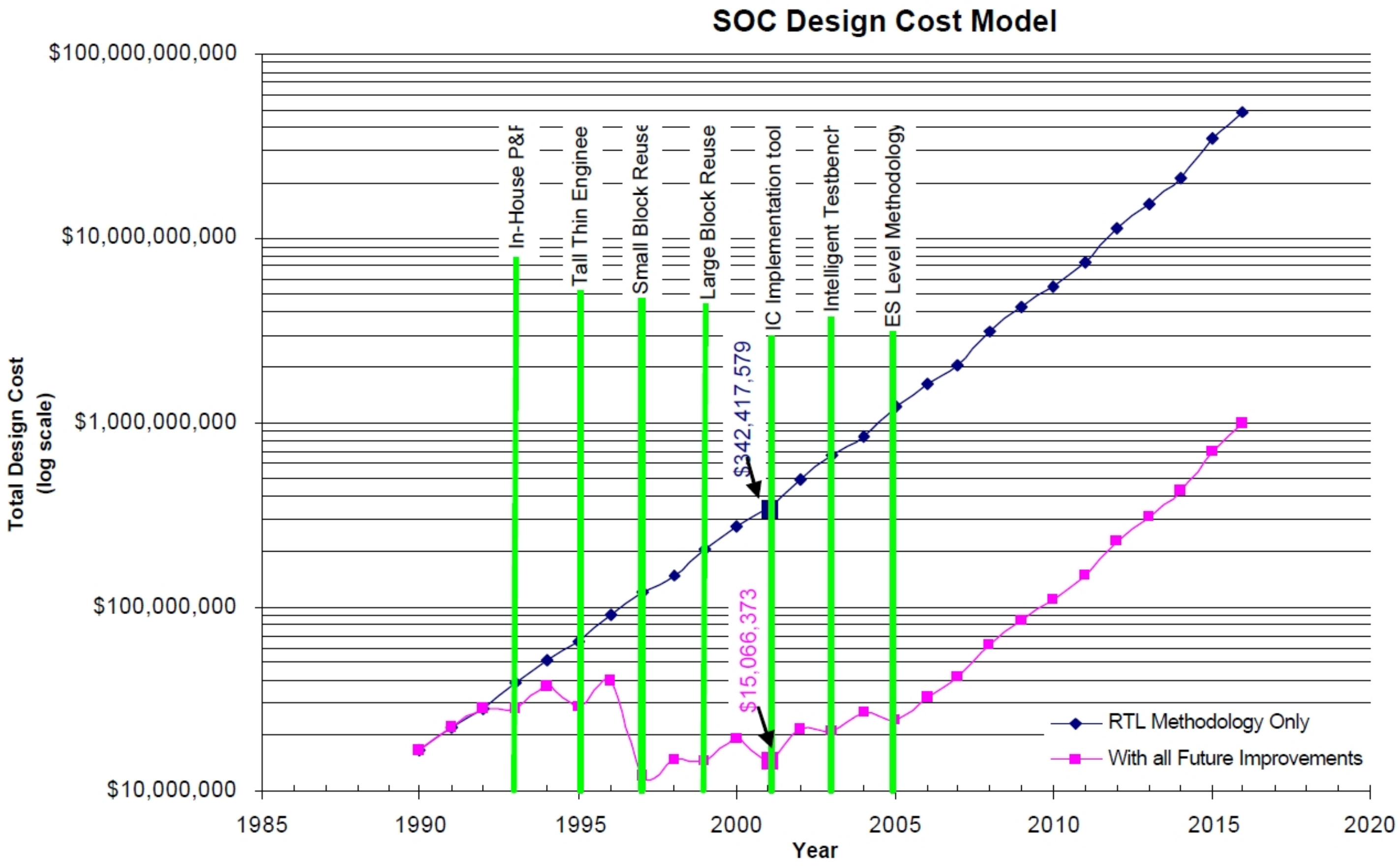
- 2001 ITRS – Predicts the main trends in the semiconductor industry spanning across 15 years into the future. The participation of experts from Europe, Japan, Korea, and Taiwan as well as the U.S.A.
- Updated every other year has improved the quality of R&D investment decisions made at all levels. Most of all, it has provided useful guidance for supplier of equipment, material and software. It has also provided clear targets for research and helped channel research efforts to areas that truly need research breakthroughs.
- 2012 – IEEE Rebooting Computing Initiative
- 2016 – IEEE International Roadmap for Devices and Systems (IRDS)

INTERNATIONAL ROADMAP FOR DEVICES AND SYSTEMS

Ref: International Technology Roadmap for Semiconductors (ITRS), http://www.itrs2.net/
Ref: International Roadmap for Devices and Systems (IRDS), https://irds.ieee.org/
Ref: Conte, Thomas M., et al. "Rebooting computing: The road ahead." Computer 50.1 (2017): 20-29.
Ref: Gargini, Paolo A. "The global route to future semiconductor technology." IEEE circuits and devices magazine 18.2 (2002): 13-17.

2001 ITRS Design Cost Model

- Improvements in product since RTL Methodology.
  - In-House Place & Route
  - The Tall Thin Engineer
  - Small Block Reuse
  - Large Block Reuse
- Planned improvements
  - IC Implementation Tool Set;
  - Intelligent Test Bench
  - ES Level Methodology

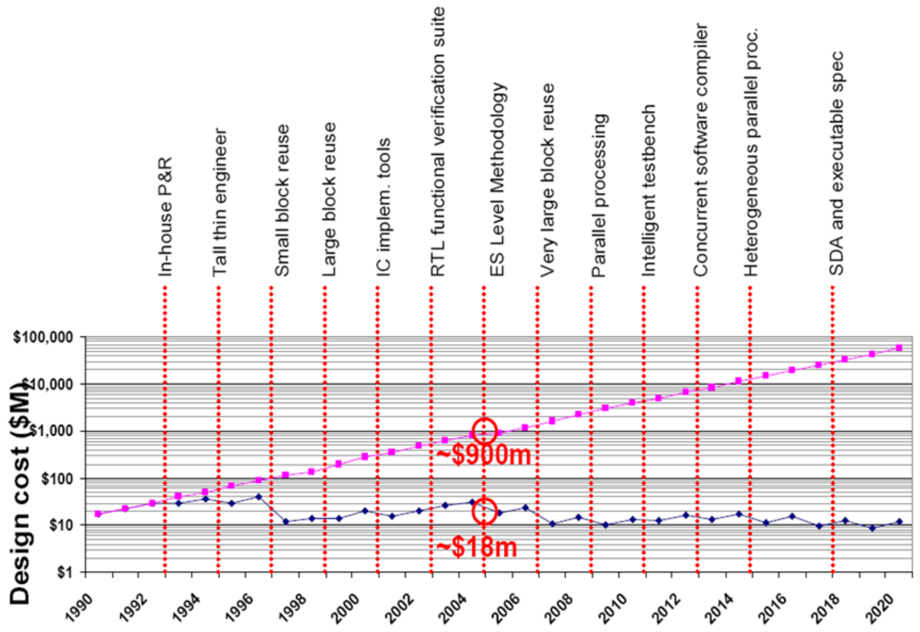


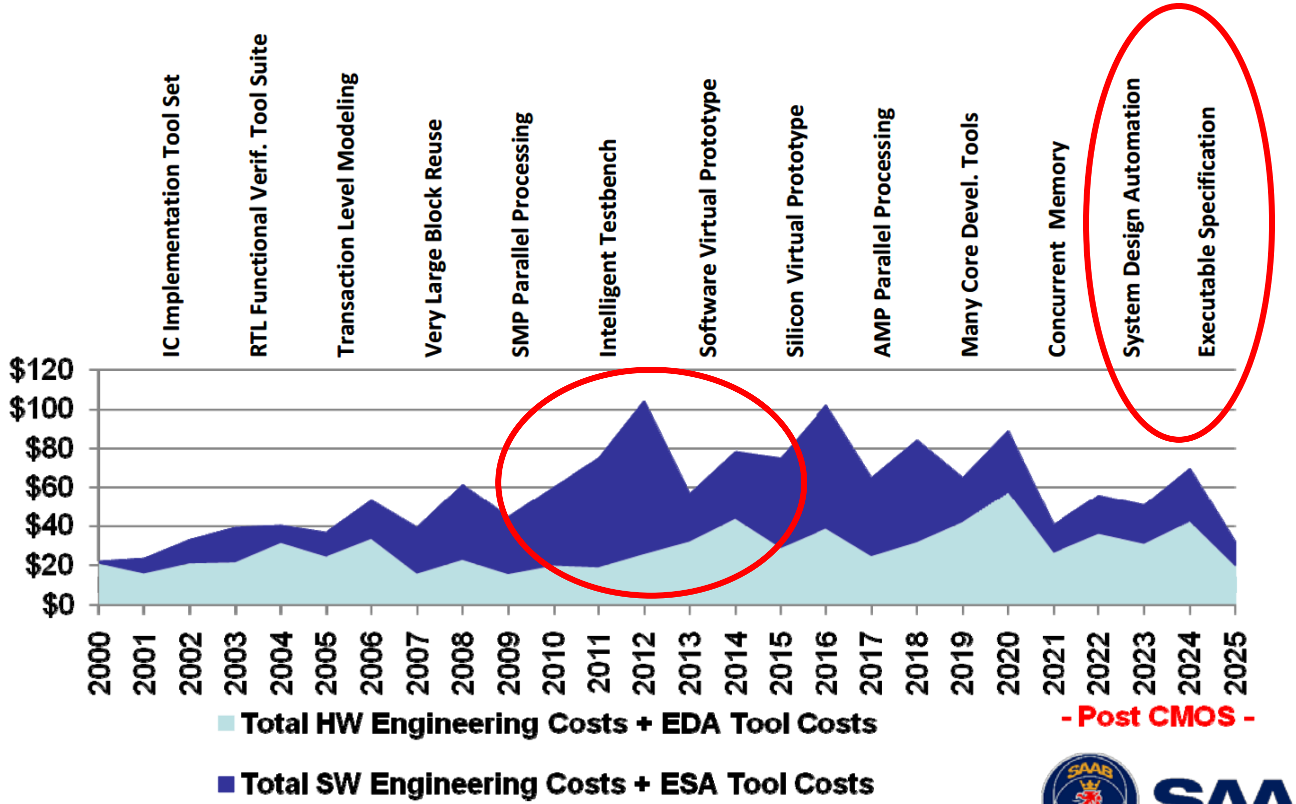
Ref: ITRS 2001 Design Chapter, http://www.itrs2.net/

Ref: Smith, Gary. "Updates of the ITRS design cost and power models." *2014 32nd IEEE International Conference on Computer Design (ICCD)*. IEEE, 2014

The Complexity Challenge … *Embedded software design*

- ES level methodology: Level above RTL, including both HW and SW design.
  True system-level design (SDA and executable Specification) including HW, SW, mechanical, opto, etc. This would represent a shift in methodology equal in impact to the introduction of the register-transfer level (RTL) methodology in the late 1980s.





Ref: ITRS 2005 Design chapter (left), http://www.itrs2.net/
Ref: ITRS 2010 Design chapter (right), http://www.itrs2.net/

Avionics – Explosion in software complexity

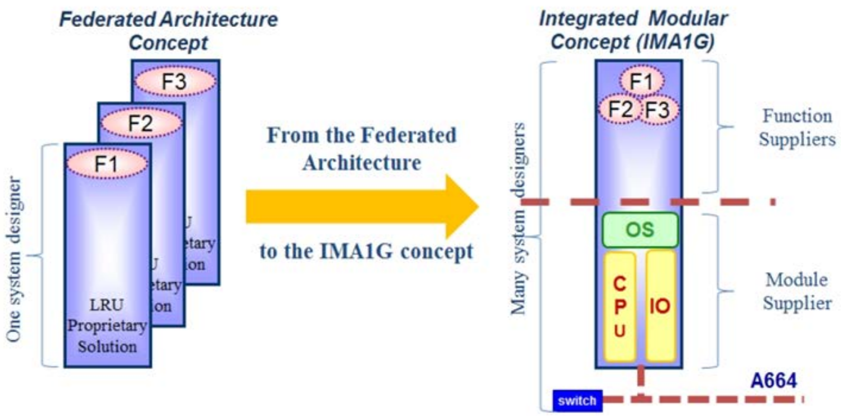
Saab early principle: System computer for integration

~ 1967 AJ37, 1 computer

~ 1974 JA37, 5 computers

~ 1988 JAS39, 40 computers

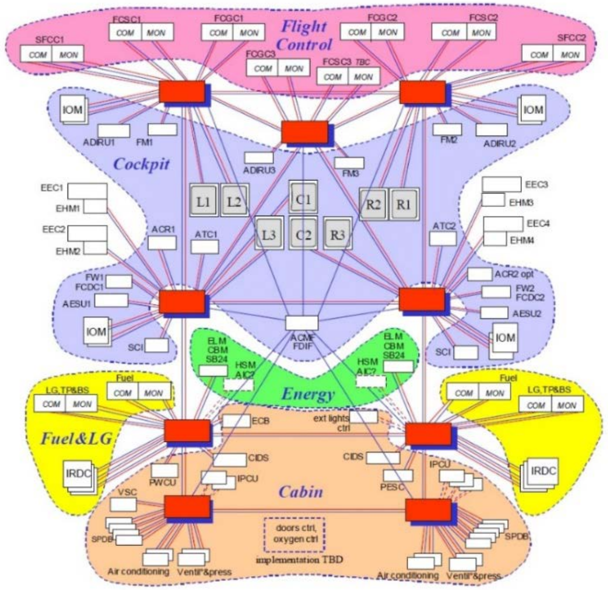
~ 1990 Integrated Modular Avionics (IMA) replaces "federated architecture" principle: "one function - one computer".



IMA enabler Deterministic behaviour !

- ARINC 653 – time and space separated partitioned applications
- ARINC 664 – latency bounded switched Ethernet communication
- RTCA DO-297 nov. 2005 – Certification Considerations

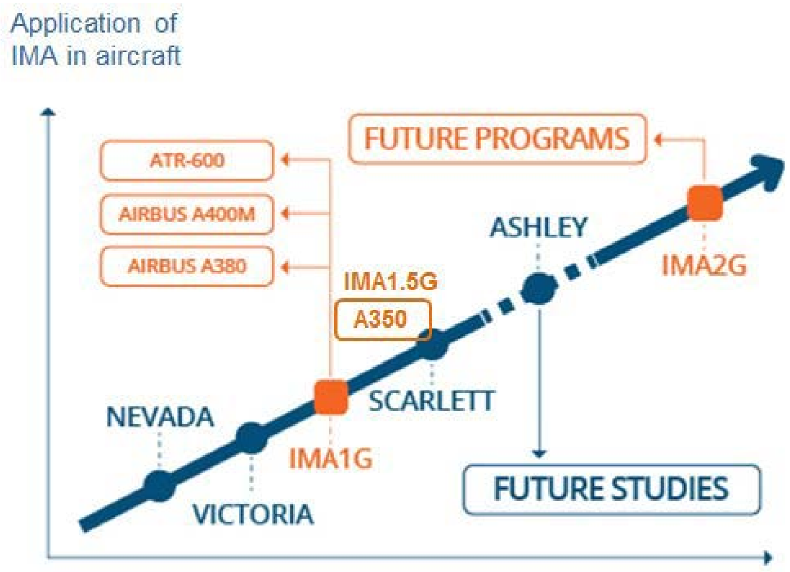
~ 2005 Airbus 380 followed by Boeing 787



Ref: ASHLEY, www.ashleyproject.eu/
Ref: Butz, Henning. "Open integrated modular avionic (ima): State of the art and future development road map at airbus deutschland." (2010)

Architecture trend (evolution)

- EU FP7
  - SCARLETT 2008-2012
  - ASHLEY 2013-2017

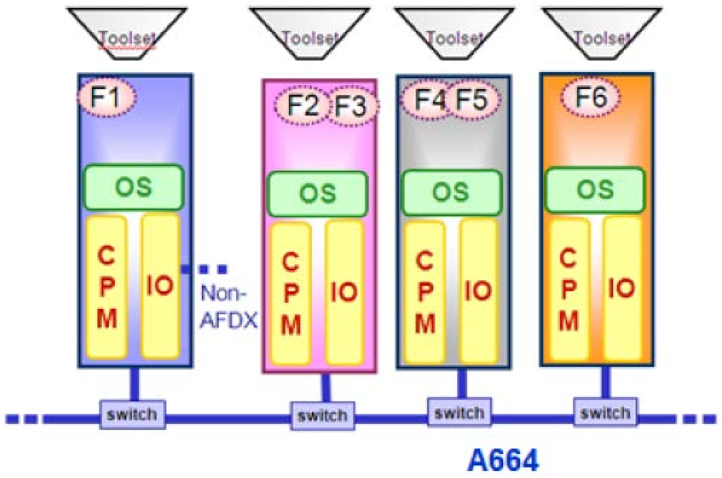


Ref: SCARLETT, www.scarlettproject.eu/
Ref: ASHLEY, www.ashleyproject.eu/

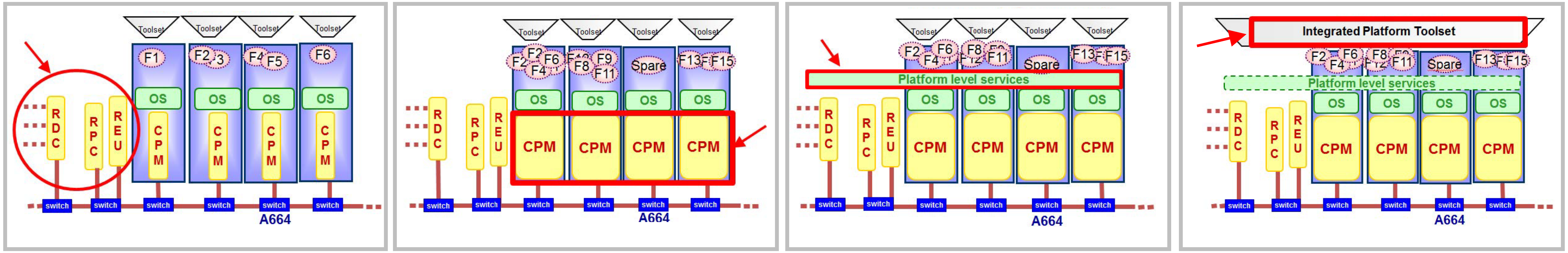
IMA 1G to IMA 2G

- *Separating I/O from computing modules*
- *Increasing computing module performance*
- *Providing platform-level services (e.g. DB service)*
- *Integrating processes and tools*

From IMA 1G …



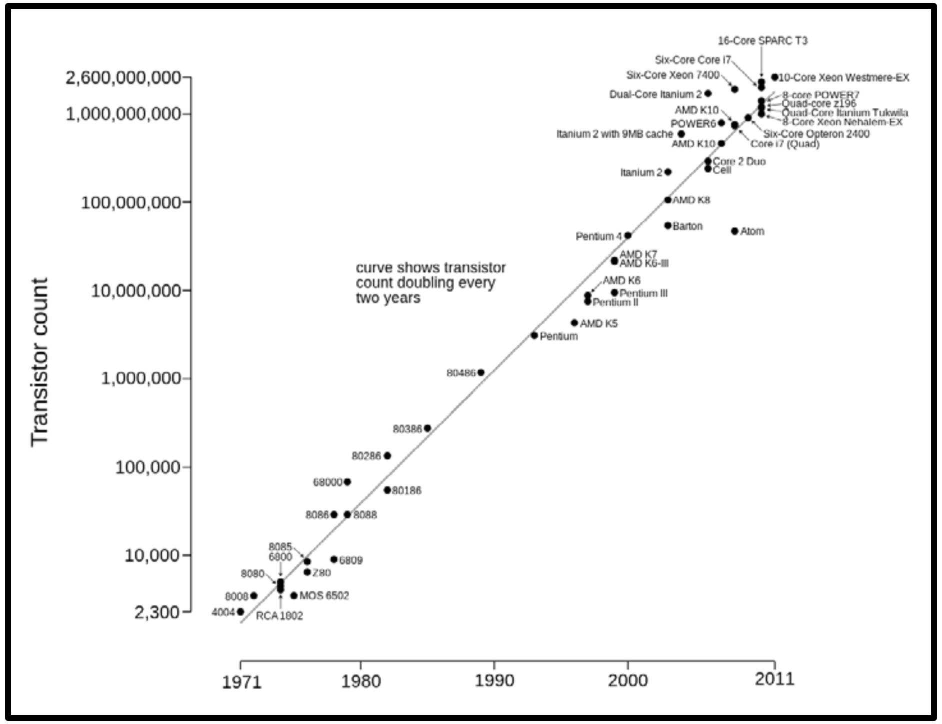
… to IMA 2G - Distributed Modular Electronics

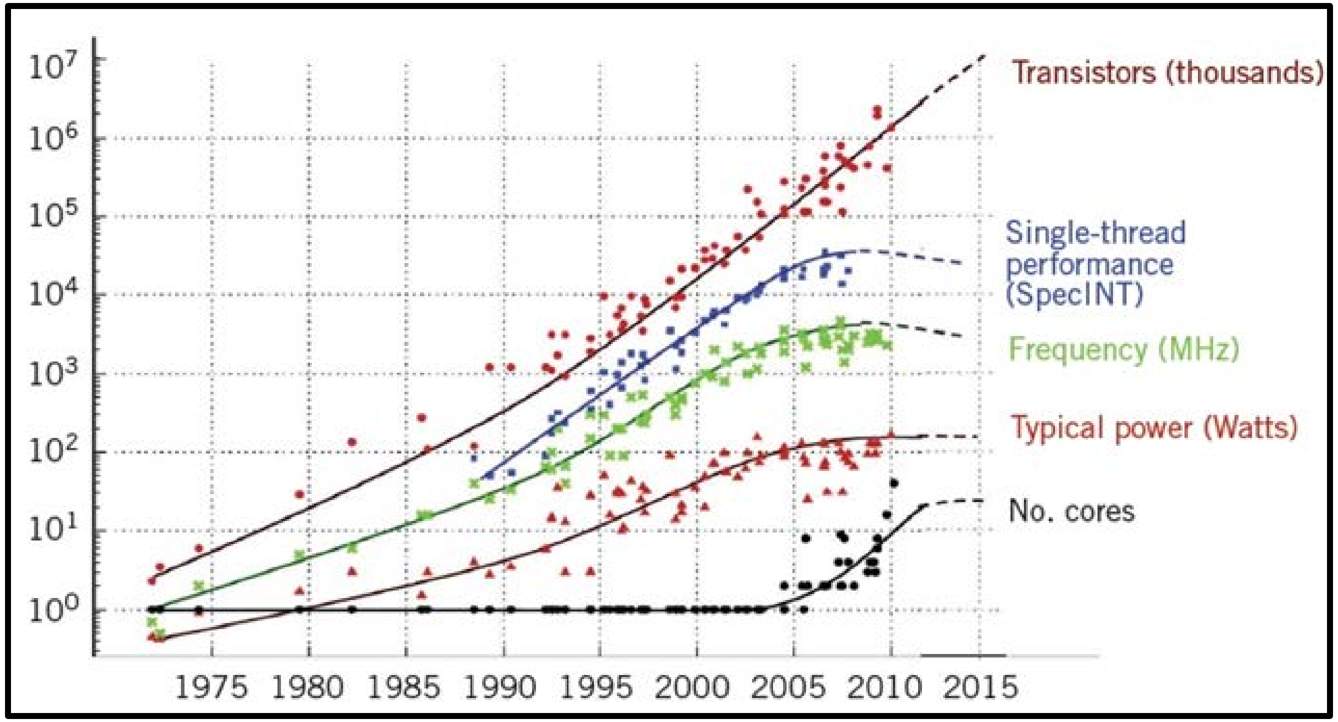


Ref: ASHLEY (Avionics Systems Hosted on a distributed modular electronics Large scale dEmonstrator for multiple tYpes of aircraft), www.ashleyproject.eu/

Historic trend in software systems

For decades enhanced CPU performance – forgiving wasteful software technology



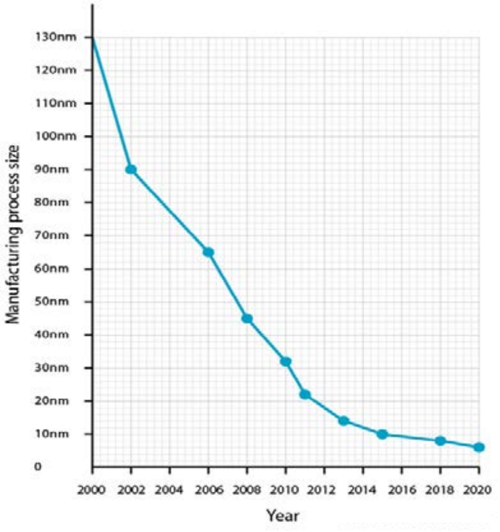


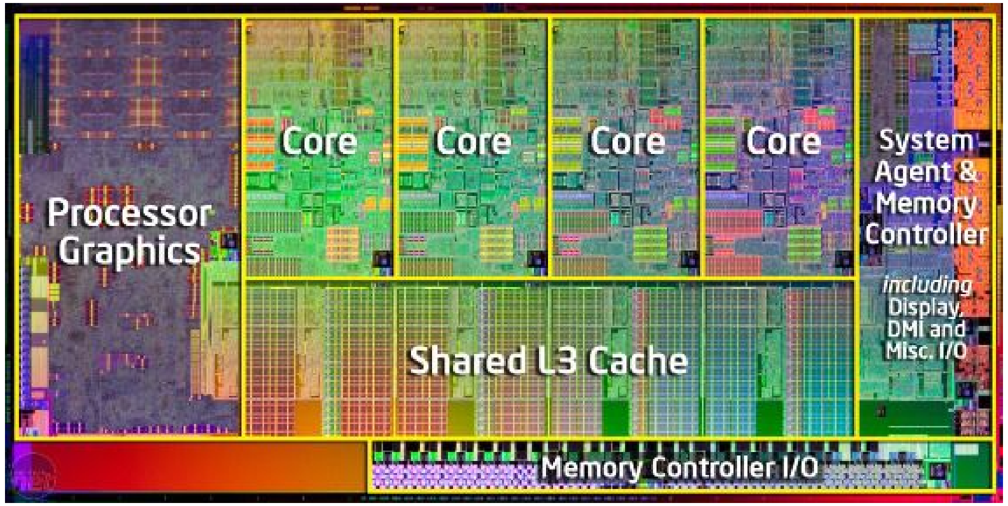
Ref: http://phys.org/news/2015-04-silicon-valley-years-law.html

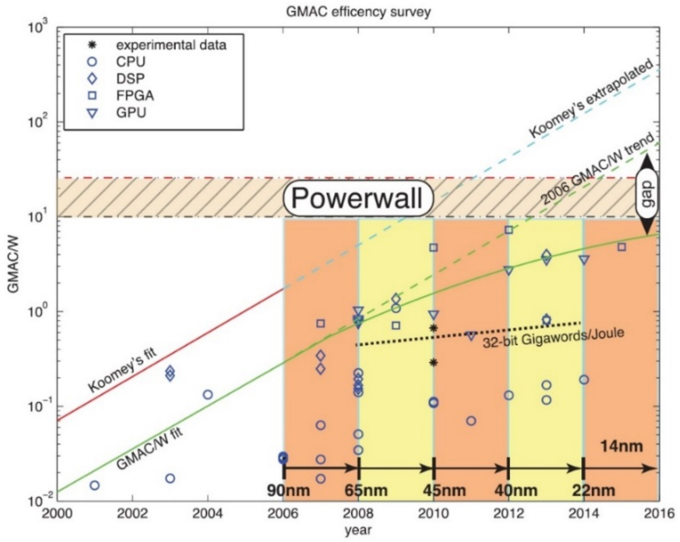
Ref: Naffziger, Samuel. "Technology impacts from the new wave of architectures for media-rich workloads." VLSI Technology (VLSIT), 2011 Symposium on. IEEE, 2011.

Evolutionary CPU/Software scaling

- Feature Scaling (Technology node) – Limited by cost and atom size
- Frequency scaling – Network data transport - Limited by speed of light
- Multicore scaling – Limited by power and shared cache access – shared resources





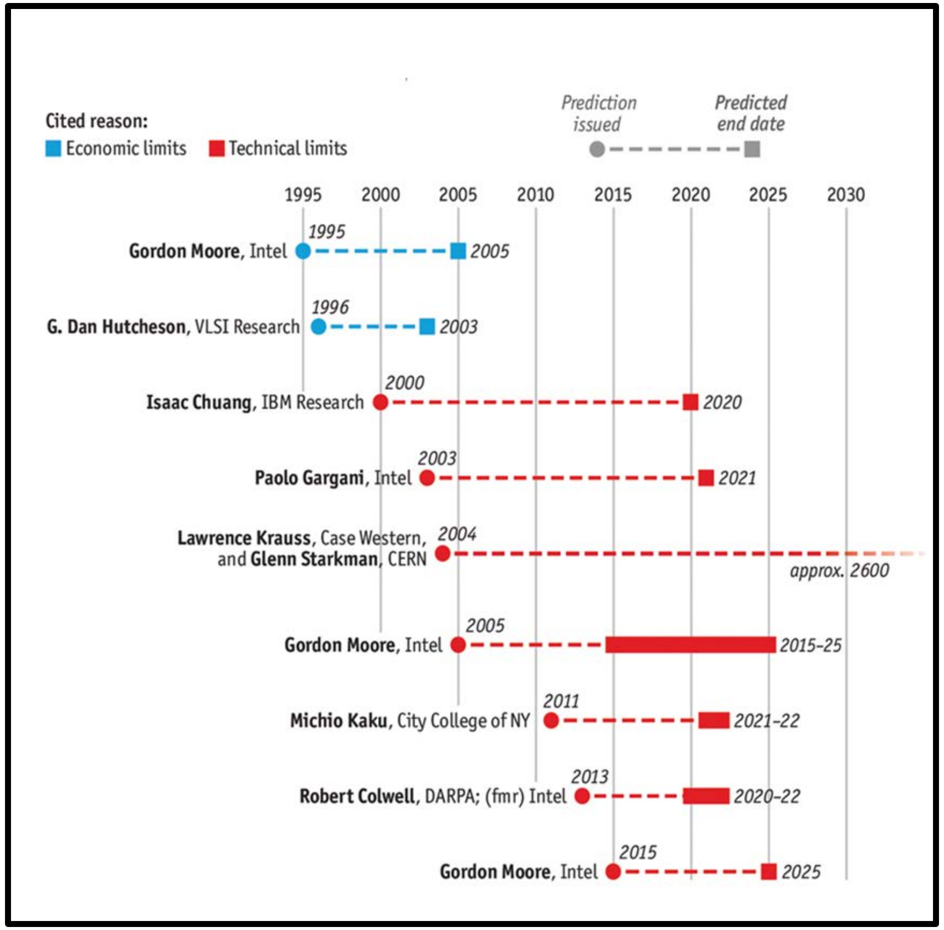


Ref: http://www.futuretimeline.net/subject/computers-internet.htm

Ref: Degnan, B., Marr, B. & Hasler, J. "Assessing trends in performance per watt for signal processing applications." IEEE Transactions (2016)

MOORE’S LAW – is dead !

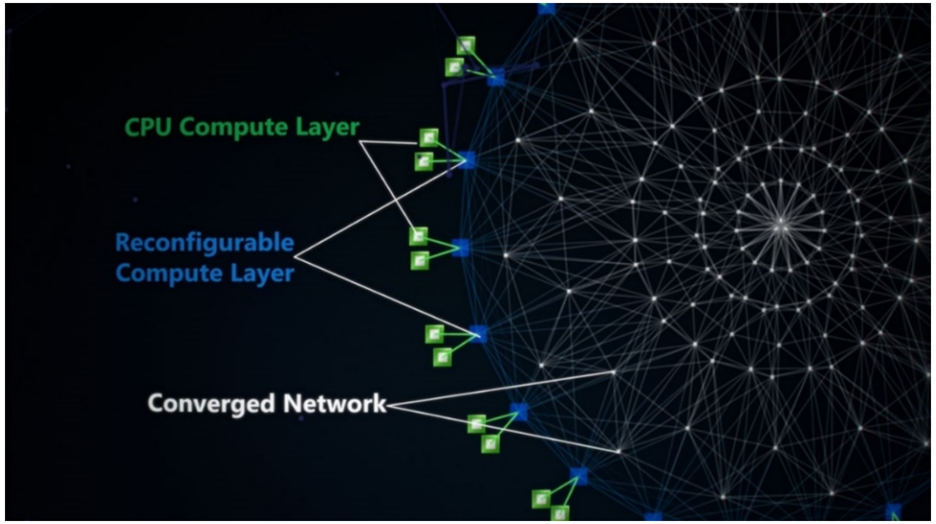
- Economic limit is reached !
- The question is not how many transistors can be squeezed onto a chip, but how many chips can be fitted economically into a warehouse (datacenter or cloud)
- Moore's law itself is irrelevant.
- Non - von Neumann computing !!!
  - Highly parallel software
  - New software algorithms
  - New software languages
  - System software

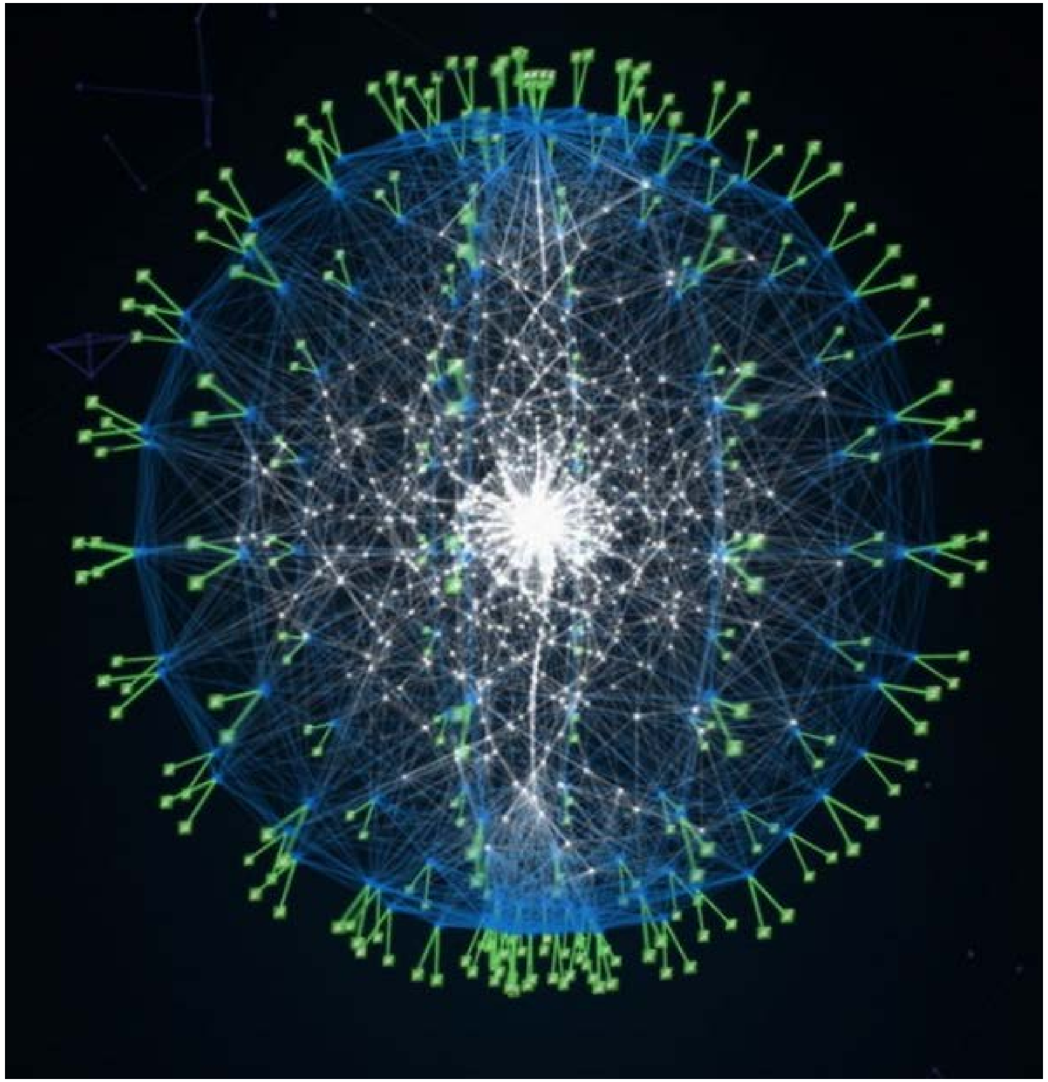


Ref: http://www.economist.com/blogs/economist-explains/2015/04/economist-explains-17
Ref: Conte, Thomas M., et al. "Rebooting computing: The road ahead." *Computer* 50.1 (2017): 20-29.

Microsoft intelligent cloud

- Needed for AI serving in real time
- Deep Neural Network (DNN) processor
  - FPGA technology
  - Reconfigurable computing



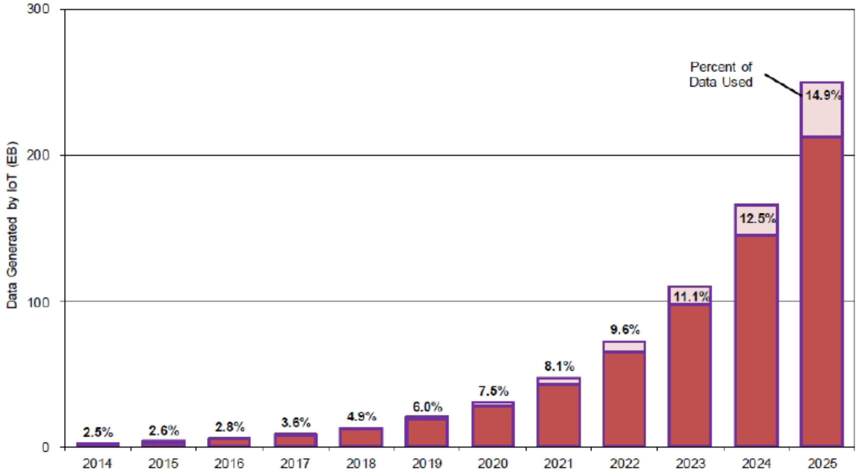


Ref: https://www.microsoft.com/en-us/research/project/project-catapult/

Ref: Fowers, Jeremy, et al. "A Configurable Cloud-Scale DNN Processor for Real-Time AI." *2018 ACM/IEEE 45th Annual International Symposium on Computer Architecture (ISCA)*. IEEE, 2018.

Cyber-Physical Systems (CPS)

- Combination of Tactile Internet, Internet of Things and 5G vision.
  - 1 ms roundtrip latency
  - Edge computing
- The adoption of IoT devices depends on the use we can make of data



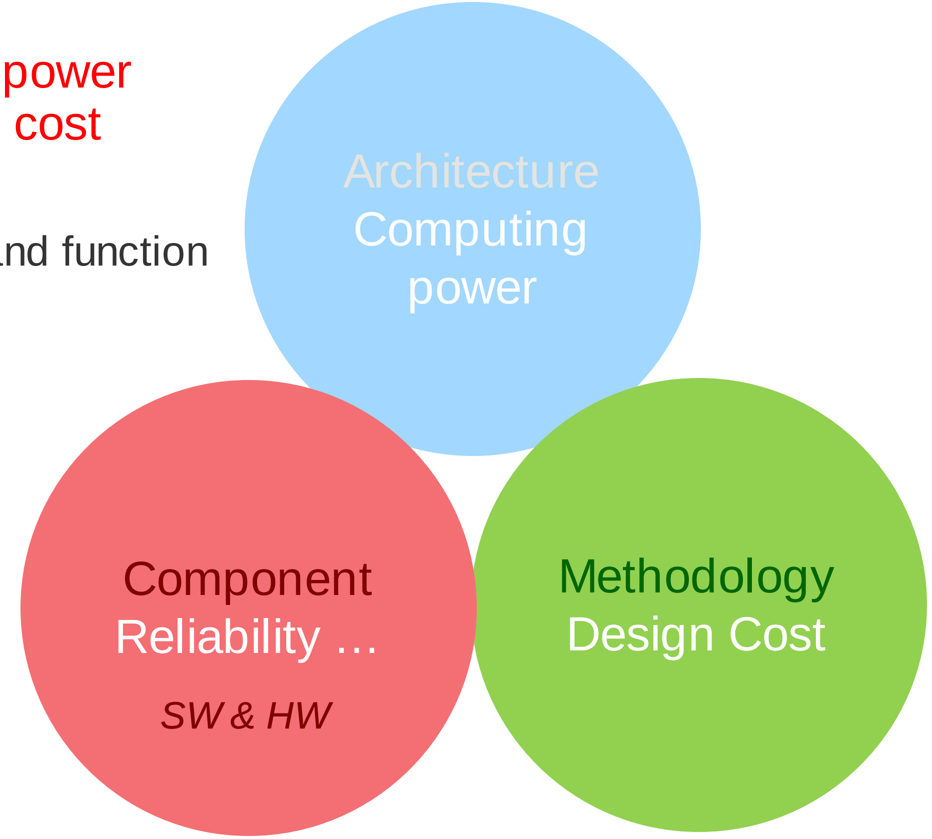
Ref: Maier, Martin, et al. "The tactile internet: vision, recent progress, and open challenges." IEEE Communications Magazine 54.5 (2016): 138-145.
Ref: E. Macii, M. Grosso, M. Poncino, Power Efficiency in the Design of IoT Devices, DATE Tutorial Dresden, Germany – 3/14/2016

Long term industry need

Future products will have increased functionality and level of automation, including autonomous operation and management of air vehicles (manned or unmanned)

This will directly depend on reliable and increasing computing power in the system, together with predictable development time and cost

- Architectures and principles for performance scaling, technology and function
  - Introduction of next generation Integrated Modular Avionics (IMA2G)
  - Run-time reconfigurable architectures
- Resilient, security and reliability related challenges to meet safety
  - Aging and radiation-induced soft errors
  - Architecture mitigation techniques
- Cost effective design methodology
  - Correct-by-construction design flow based on formal methods
  - Automated and power efficient software generation

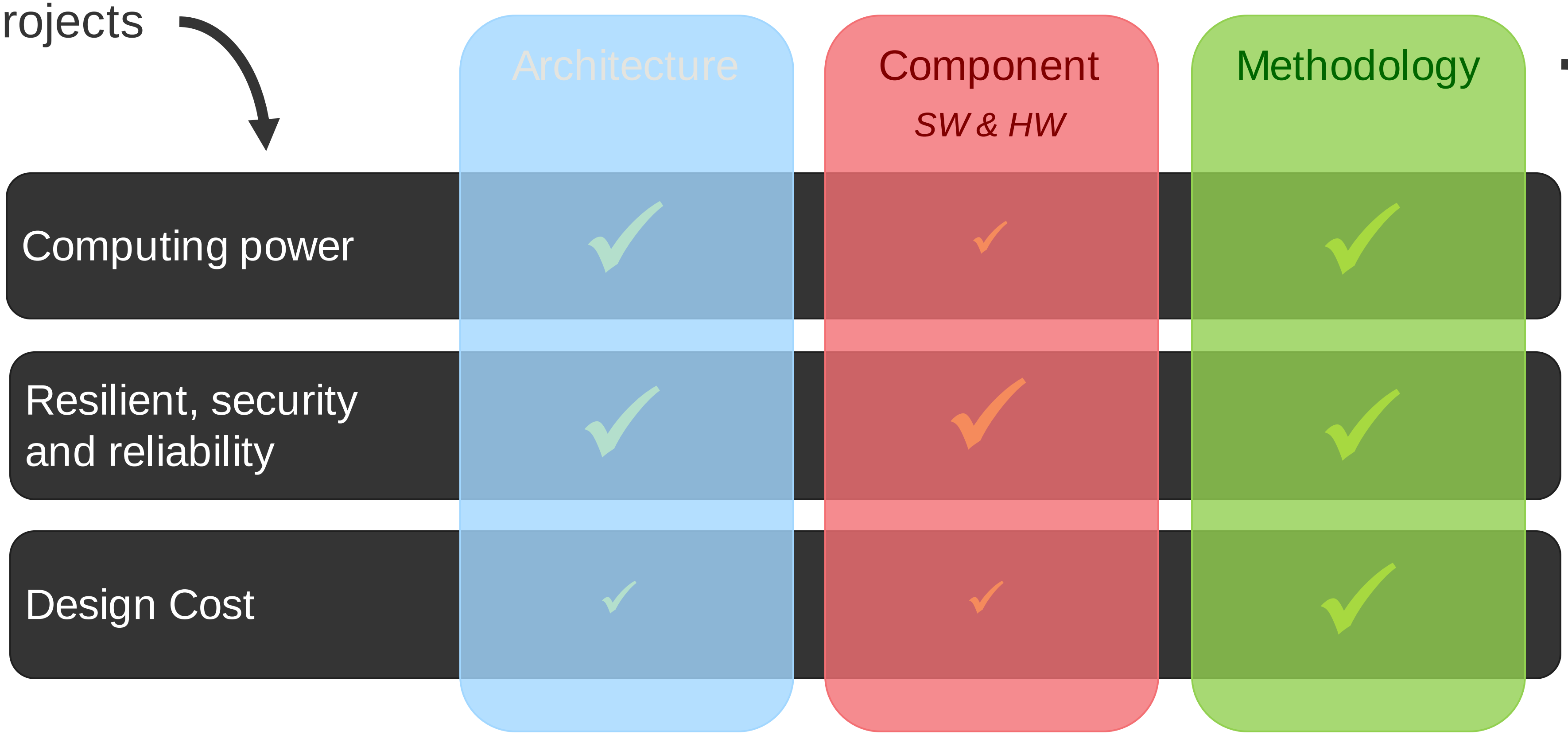


Strategy

"The performance of a system is not controlled by the individual components, but by the way that you can assemble these different components," said **Paolo Gargini**, head of the International Roadmap for Devices and Systems, an IEEE Standards Association Industry …

Overall focus area and approach for R&T projects

Of today will be obsolete tomorrow …



Architecture & methodology will be used together with components of tomorrow e.g. 2028 !!

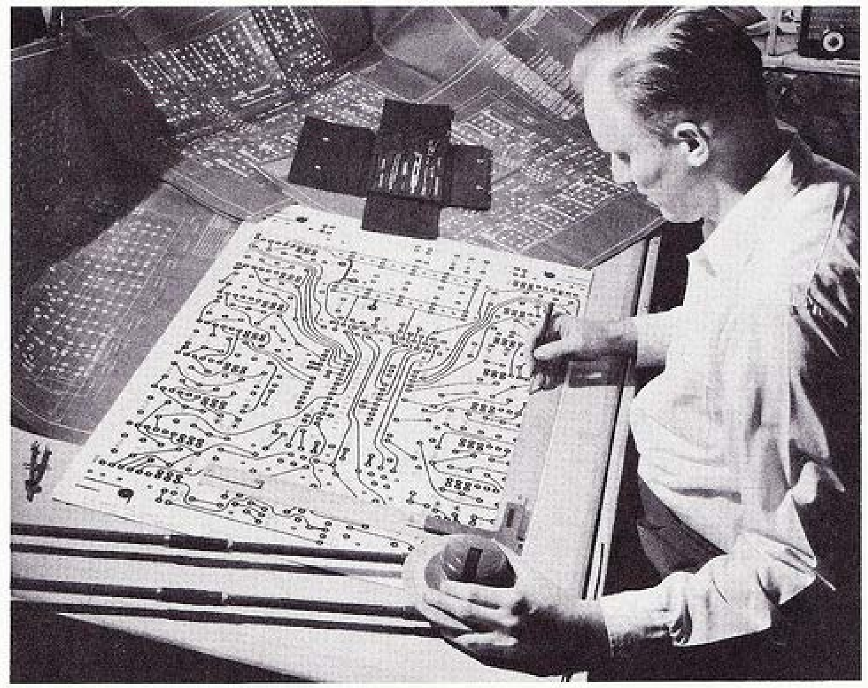
Challenges/expectations on Castor

1. Contribute to flat system development cost (ITRS cost model) as well as IRDS roadmap.
    - By developing software methodology (that can be automated at later stage)
2. Develop software design and verification methodology that guarantee full function and performance at first/each product deployment (no update and/or bug fix allowed)
3. Follow international progress, assess findings and contribute to methodology for:
    - System Design Automation (SDA) and Executable Specification
    - Software System Complexity
4. Understand industry safety concerns for determinism and use of shared resources.
5. Build up domain knowledge/understanding for relevant industrial environmental needs (not develop the products), including safety, security and certification requirement.
6. Cooperate with teams outside the center to understand the ”complete big picture for AI”.

Ref: Hanyan, Li, et al. "Software complexity measurement based on complex network." Software Engineering and Service Science (ICSESS), 2017 8th IEEE International Conference on. IEEE, 2017.

The potential for innovations is gigantic !

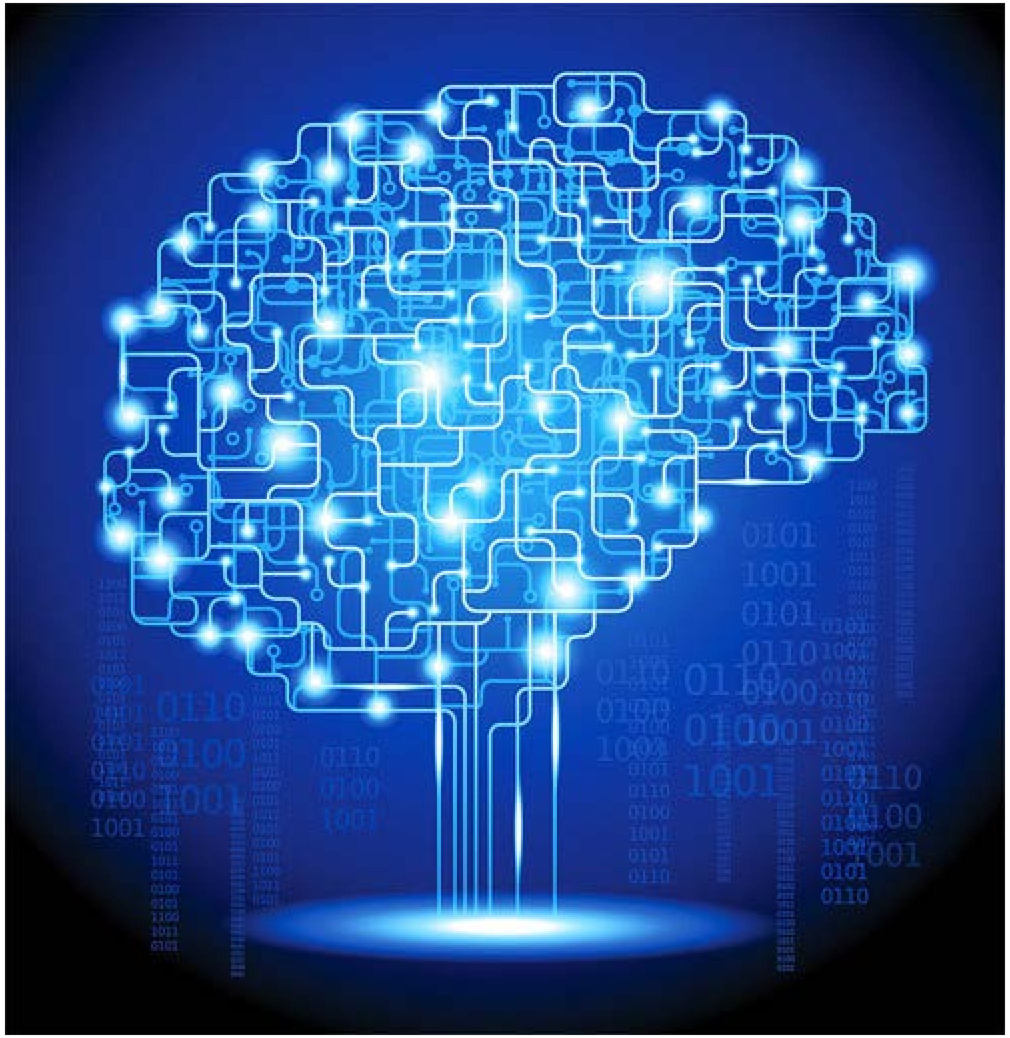
- Is Software maturity for design and verification today where hardware were at 1960’s ?? Artistic software architecture … UML boxes and arrows … Manual code inspection …



Ref: https://www.evilmadscientist.com/2013/how-printed-circuit-boards-are-designed-1960-edition/
Ref: http://www.computerhistory.org/revolution/digital-logic/12/287

Summary

- **Research and education** in software technology, software and hardware components and related engineering skills is a central and strategically important field which Swedish industry and academia must take seriously if Swedish industry is to maintain its ambition to develop competitiveness products based on complex software in the future.
- Deep knowledge of **physical properties** of current and emerging semiconductor technology is essential.
- **Safety, security and resilience** properties of general electronics and processing platforms can be analysed based on; semiconductor physics, integrated circuit technology, low level software and applied design methodologies.
- Increased **processing power** will depend on architecture scaling and innovative system design of electronic platforms.



Thank you for your attention.
Any questions ?

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